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EXAMINER

LEE, CHRISTOPHER E

ART UNIT PAPER NUMBER

2112

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/681,446	<b>Applicant(s)</b> KOBAYASHI ET AL.	
	<b>Examiner</b> Christopher E. Lee	<b>Art Unit</b> 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-61 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-25 is/are allowed.
- 6) ☒ Claim(s) 1-7, 26-33, 35-38, 40-42, 45-51 and 54-61 is/are rejected.
- 7) ☒ Claim(s) 8-11, 34, 39, 43, 44, 52 and 53 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 July 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the Amendment filed on 12<sup>th</sup> of July 2006. Claims 1, 4, 5, 8, 11-16, 19-22, 31, 36, 38, 40, 41, 43, and 58 have been amended; no claim has been canceled;  
5 and no claim has been newly added since the Non-Final Office Action was mailed on 10<sup>th</sup> of April 2006. Currently, claims 1-61 are pending in this Application.

### *Specification*

2. The following guidelines illustrate the preferred layout for the specification of a utility  
10 application. These guidelines are suggested for the applicants' use.

### **Arrangement of the Specification**

- 15 As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- 20 (a) TITLE OF THE INVENTION.  
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.  
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.  
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT  
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT  
25 DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or  
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a).  
"Microfiche Appendices" were accepted by the Office until March 1, 2001.)  
30 (f) BACKGROUND OF THE INVENTION.  
(1) Field of the Invention.  
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.  
(g) BRIEF SUMMARY OF THE INVENTION.  
35 (h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).  
(i) DETAILED DESCRIPTION OF THE INVENTION.  
(j) CLAIM OR CLAIMS (commencing on a separate sheet).  
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).  
40 (l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino

acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

In this case, the specification does not arrange BRIEF SUMMARY OF THE INVENTION before BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS on page 4.

- 5     3.     The disclosure is objected to because of the following informalities:

Substitute "signal" by --single-- in line 7 on page 7, paragraph [0023].

Appropriate correction is required.

### ***Response to Amendment***

- 10     4.     The Amendment document in the Response is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121, as amended on June 30, 2003 (*See 68 Fed. Reg. 38611*, Jun. 30, 2003). In fact, the claim status of the claim 58 is not (Original), but (Currently Amended). See MPEP 714 [R-3] and 37 CFR 1.121(c).

### ***Claim Objections***

15

5.     Claim 31 is objected to because of the following informalities:

It recites the subject matter "the first SMI handler" in line 6. However, it has not been specifically clarified in the claim 31 and its intervening claims. Therefore, the Examiner presumes that the term "the first SMI handler" could be considered as --the SMI handler-- in  
20 light of the specification since it is not defined in the claims.

And, it also recites the subject matter "the second SMBase" in line 6. However, it has not been specifically clarified in the claim 31 and its intervening claims. Therefore, the Examiner presumes that the term "the second SMBase" could be considered as --the second SMBase address-- in light of the specification since it is not defined in the claims.

25

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

5 (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1, 3-5, 45, and 47-49 are rejected under 35 U.S.C. 102(a) as being anticipated by Dale [GB 2 382 180].

10 Referring to claim 1, Dale discloses a method (i.e., a method for waking up components in a dual-processor based system; See Abstract) comprising:

- receiving a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF\_Module 340 receiving RF\_RADIO\_ON signal 370 in Fig. 3; See page 18, lines 6-11);
- 15 • handling the first SMI (i.e., said initiating signal for waking up process) with a first processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines 15-23);
- generating a wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) with the first processor (in fact, said interrupt signal was caused by said RF\_RADIO\_ON signal from said GSM Processor; See page 18, lines 27-30);
- 20 • awakening a second processor (i.e., said MMI Processor), based on the wake-up signal (i.e., said interrupt signal) from the first processor (See page 18, lines 30-31), wherein
  - the wake-up signal (i.e., said interrupt signal for waking up MMI Processor) references (i.e., fetches) a first memory address of a default SMI handler (i.e., memory element having instructions in Memory 350 in Fig. 3, which is executed
- 25 by said GSM Processor at Step 490 in Fig. 4; See page 21, lines 9-14); and

- handling the first SMI (i.e., said waking up process) with the second processor (See page 19, lines 1-4).

*Referring to claim 3, Dale teaches*

- 5
- the first and second processors (i.e., GSM 312 and MMI 322 Processors in Fig. 3) are physical processors (See page 12, lines 5-6, and 15).

*Referring to claim 4, Dale teaches that handling the first SMI (i.e., initiating signal for waking up process) with a first processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines*

10 15-23) comprises:

- executing the default SMI handler (i.e., instructions being executed by said GSM Processor at Step 490 in Fig. 4) located at the first memory address (i.e., memory element having said instructions in Memory 350 in Fig. 3; See page 21, lines 9-14).

15 *Referring to claim 5, Dale teaches*

- the wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) is a startup inter processor interrupt SIPI signal (See page 18, line 27 through page 19, line 4).

20 *Referring to claim 45, Dale discloses a system (i.e., cellular communication device in Fig.3) comprising:*

- a controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4,

in fact, RF\_Module 340 receiving RF\_RADIO\_ON signal 370 in Fig. 3; See page 18, lines 6-11);

- a memory (i.e., Memory 350 of Fig. 3) with a first memory address (i.e., memory element in said Memory) that contains code (i.e., waking up process; See page 20, lines 15-23);

- 5
- a first processor (i.e., GSM Processor 312 of Fig. 3) coupled to the controller hub (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3) to handle the first SMI (i.e., said waking up process), wherein

- the first processor executes the code at the first memory address and generates a wake-up signal (in fact, said interrupt signal was caused by said

10 RF\_RADIO\_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30); and

- a second processor (i.e., MMI Processor 322 of Fig. 3) coupled to the controller hub (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3) to handle the first SMI (i.e., said waking up process) after receiving the wake-up signal (See page 16, line 28 through page 17, line 2), wherein

- 15
- the second processor (i.e., said MMI Processor) executes the code at the first memory address (See page 18, lines 30-31 and page 19, lines 1-4).

*Referring to claim 47, Dale teaches*

- 20
- the first and second processors (i.e., GSM 312 and MMI 322 Processors in Fig. 3) are physical processors (See page 12, lines 5-6, and 15) located on separate packages (i.e., said GSM Processor 312 is packaged within GSM Sub-system 310, and said MMI Processor is packaged within MMI Sub-system 320 in Fig. 3; See page 12, lines 5-6, and 15).

*Referring to claim 48, Dale teaches*

- a pin (i.e., output pin from GSM ULPD 314 in Fig. 3) is toggled (i.e., RF\_RADIO\_ON signal 370 being set/reset in Fig. 3) on the controller hub (i.e., said GSM ULPD) to generated the first SMI (i.e., GSM ULPD 314 of Fig. 3 generates the SMI, which is an initiating signal for waking up process; See Steps 405-415 in Fig. 4).

*Referring to claim 49, Dale teaches*

code (i.e., Steps 405-415 in Fig. 4) is executed by the controller hub (i.e., GSM ULPD 314 of Fig. 3) to generate the first SMI (i.e., said GSM ULPD generates the SMI, which is an initiating signal for waking up process; See page 18, lines 6-14).

8. Claims 26-33, 35-38, 54-59, and 61 are rejected under 35 U.S.C. 102(b) as being anticipated by Nguyen et al. [US 2002/0099893 A1; hereinafter Nguyen].

*Referring to claim 26, Nguyen discloses a method (i.e., method for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:*

- receiving an system management interrupt (i.e., all the processors receiving SMI; See paragraph [0017], lines 15-20);
- executing a SMI handler (e.g., Operating code for SMI handler of Processor 12c in Fig. 1) to handle a SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) for a first processor (i.e., Processor 12c of Fig. 1; in fact, said Operating code for SMI handler of Processor 12c could process said received SMI for said Processor 12c itself in Fig. 1; See paragraphs [0005] and [0018]); and

- executing the SMI handler (i.e., said Operating code for SMI handler of Processor 12c in Fig. 1) to handle the SMI (i.e., said SMI issued by chipset) for a second processor (e.g., Processor 12b of Fig. 1; in fact, said Operating code for SMI handler of Processor 12c could execute said received SMI for SMI initiating Processor 12b using parameters for said Processor 12b in Fig. 1; See paragraph [0018]).

*Referring to claim 27, Nguyen teaches*

- the SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) is a software generated SMI (i.e., software SMI; See paragraph [0017], lines 21 through 27).

*Referring to claim 28, Nguyen teaches*

- the first processor (i.e., Processor 12c of Fig. 1) executes the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) to handle the SMI (i.e., SMI issued by chipset; See step 46 in Fig. 2) for the first and the second processor (i.e., Processor 12c and Processor 12b in Fig. 1; See paragraphs [0005] and [0018]).

*Referring to claim 29, Nguyen teaches*

- the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) is located at a first memory address (i.e., memory location for said Operating code; See paragraphs [0005] and [0019]).

*Referring to claim 30, Nguyen teaches*

- the first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) is a default offset (i.e., a predetermined address at said memory

location of said Operating code) from a first system management base (SMBase) address (i.e., a starting address of SMRAM space 84 in Fig. 3) for the first processor (i.e., said Processor 12c of Fig. 1, in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

*Referring to claim 31*, Nguyen teaches executing the SMI handler (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) to handle the SMI (i.e., SMI issued by chipset) for the second processor (i.e., Processor 12b of Fig. 1; See paragraph [0018]) comprises:

- changing a target SMBase of the SMI handler from the first SMBase address (i.e., SMRAM space 84 in Fig. 3) to a second SMBase address for the second processor (i.e., SMRAM space 82 of Fig. 3 for Processor 12b of Fig. 1); and
- executing the SMI handler using the second SMBase address as the target SMBase (See paragraphs [0018]-[0020]).

*Referring to claim 32*, Nguyen discloses a method (i.e., method for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- executing system management interrupt (SMI) code (e.g., Operating code for SMI handler of Processor 12c in Fig. 1) with a first processor (i.e., said Processor 12c of Fig. 1) to handle a SMI (i.e., SMI issued by chipset initiated by peripheral devices, e.g., keyboard, etc.) for the first processor (in fact, said Operating code for SMI handler of Processor being executed for said initiating peripheral device; See paragraphs [0005] and [0006]);

- checking if the SMI is a software generated SMI (i.e., if the SMI issued by chipset initiated by a Processor; See step 46 in Fig. 2, in fact, software SMI; See paragraph [0017], lines 21 through 27; actually, checking SMI signature in SMRAM 78 of Fig. 3); and

- 5
- executing the SMI code (i.e., said Operating code for SMI handler) to handle the SMI for a second processor (i.e., Processor 12b of Fig. 1), if the SMI is software generated (See paragraph [0018], lines 13-28).

*Referring to claim 33, Nguyen teaches*

- 10
- the first processor (i.e., Processor 12c of Fig. 1) executes the SMI code (i.e., Operating code for SMI handler of said Processor 12c in Fig. 1) to handle the SMI for the second processor (i.e., SMI issued by chipset, which has been initiated by Processor 12b in Fig. 1; See steps 40-46 in Fig. 2), if the SMI is software generated (i.e., after checking SMI signature in SMRAM 78 of Fig. 3).

15

*Referring to claim 35, Nguyen teaches*

- the first processor (i.e., Processor 12c in Fig. 1) has a first system management base (SMBase) address (i.e., address of SMRAM space 84 in Fig. 3).

20

*Referring to claim 36, Nguyen teaches*

- the second processor (i.e., Processor 12b in Fig. 1) has a second SMBase address (i.e., address of SMRAM space 82 in Fig. 3).

*Referring to claim 37, Nguyen teaches*

- said SMI code (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) is located at first memory location (i.e., memory location for said Operating code), which has an offset (i.e., a predetermined address at said memory location of said Operating code) from a first SMBase address (i.e., from a starting address of SMRAM space 84 in Fig. 3; in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

Referring to claim 38, Nguyen teaches executing said SMI code (i.e., said Operating code for SMI handler) to handle the SMI for the second processor (See paragraph [0018], lines 13-28) comprises:

- changing a target SMBase from the first SMBase (i.e., SMRAM space 84 in Fig. 3) to the second SMBase (i.e., SMRAM space 82 of Fig. 3 for Processor 12b of Fig. 1); and
- executing the SMI code using the second SMBase as the target SMBase (See paragraphs [0018]-[0020]).

Referring to claim 54, Nguyen discloses an system (i.e., system for handling of system management interrupts in a multiprocessor computer system; See Abstract) comprising:

- a memory (i.e., SMRAM memory space 78 in Fig. 3) with a first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) having system management interrupt (SMI) code (i.e., said Operating code; See paragraphs [0005] and [0019]);
- a first processor (i.e., said Processor 12c of Fig. 1) to execute the SMI code when a SMI (i.e., SMI issued by chipset initiated by peripheral devices, e.g., keyboard, etc.) is

received (in fact, said Operating code for SMI handler of Processor being executed for said initiating peripheral device; See paragraphs [0005] and [0006]); and

- a second processor (i.e., Processor 12b of Fig. 1) to execute the SMI code (See paragraph [0018], lines 13-28), if the SMI is software generated (i.e., if the SMI issued by chipset initiated by a Processor; See step 46 in Fig. 2, in fact, software SMI; See paragraph [0017], lines 21 through 27; actually, checking SMI signature in SMRAM 78 of Fig. 3).

*Referring to claim 55, Nguyen teaches*

- the first processor (i.e., Processor 12c in Fig. 1) has a first system management base (SMBase) address (i.e., address of SMRAM space 84 in Fig. 3).

*Referring to claim 56, Nguyen teaches*

- the second processor (i.e., Processor 12b in Fig. 1) has a second SMBase address (i.e., address of SMRAM space 82 in Fig. 3).

*Referring to claim 57, Nguyen teaches*

- the first memory address (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) has an offset (i.e., a predetermined address at said memory location of said Operating code) from the first SMBase (i.e., from a starting address of SMRAM space 84 in Fig. 3; in fact, said Processor 12c is designated as default SMI handling processor, wherein said Operating code is located at said predetermined address; See paragraphs [0005], [0008], and [0019]).

*Referring to claim 58, Nguyen teaches*

- a target SMBase (i.e., memory location for Operating code for SMI handler of Processor 12c in Fig. 1) referenced by the SMI code (i.e., accessed by said Operating code), by default, (i.e., a predetermined address at said memory location of said Operating code) is the first SMBase (i.e., address of SMRAM space 84 in Fig. 3 because said Processor 12c is designated as default SMI handling processor; See paragraph [0019]).

*Referring to claim 59, Nguyen teaches*

- the target SMBase is changed to the second SMBase (i.e., from SMRAM space 84 to SMRAM space 82 in Fig. 3 for Processor 12b of Fig. 1) before the second processor (i.e., said Processor 12b) executes the SMI code (See paragraphs [0018]-[0020]; in fact, a default SMI handling Processor 12c executes Operating code for SMI handler of Processor 12b in Fig. 1, which is actually the SMI code).

*Referring to claim 61, Nguyen teaches*

- the first and second processors (i.e., Processor 12c and Processor 12b in Fig. 1) are physical processors (See paragraph [0016], lines 1-5).

### ***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 2 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 45, and 47-49 above, and further in view of Nalawadi [US 2003/0009654 A1].

*Referring to claim 2*, Dale discloses all the limitations of the claim 2, except that does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Processors), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

*Referring to claim 46*, Dale discloses all the limitations of the claim 46, except that does not teach that both the first and second processors are logical processors located on the same die.

Nalawadi discloses a computer system having a single processor equipped to serve as

5 multiple logical processors (See Abstract), wherein

- both first and second processors are logical processors located on the same die
- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors on the same die (i.e., multiple logical processors on said Intel® Pentium® 4 Processor; See paragraph [0006], lines 7-9).

10

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., GSM and MMI Sub-systems), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for

15 executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

15

12. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 45, and 47-49 above, and further in view of Rankin [US 5,613,071 A].

20

*Referring to claim 6*, Dale discloses all the limitations of the claim 6, except that does not expressly teach that the first memory address is aligned.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is aligned (See col. 14, lines 14-27).

5 Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said method (i.e., a method for waking up components in a dual-processor based system), as disclosed by Dale, for the advantage of providing support for said atomic operations on remote data through said first memory address being aligned (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

10

*Referring to claim 7, Rankin teaches*

- the first memory address (i.e., said AOM Region) is 4K aligned (See col. 14, lines 20-22).

15 13. Claims 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1].

*Referring to claim 40, Dale discloses an apparatus (i.e., cellular communication device in Fig.3) comprising:*

- a controller (i.e., GSM ULPD 314 of Fig. 3) to generate a first system management interrupt (SMI; i.e., initiating signal for waking up process; See Steps 405-415 in Fig. 4, in fact, RF\_Module 340 receiving RF\_RADIO\_ON signal 370 in Fig. 3; See page 18, lines 6-11);
  - a first logical processor (i.e., GSM Processor 312 of Fig. 3), coupled to the controller (actually, said GSM Processor being coupled to said GSM ULPD in Fig. 3), to handle the
- 20

first SMI (i.e., said waking up process) and generate a wake-up signal (in fact, said interrupt signal was caused by said RF\_RADIO\_ON signal from GSM Sub-system 310 in Fig. 3; See page 18, lines 27-30), wherein

- the wake-up signal (i.e., said interrupt signal for waking up MMI Processor) references (i.e., fetches) a first memory address of a default SMI handler (i.e., memory element having instructions in Memory 350 in Fig. 3, which is executed by said GSM Processor at Step 490 in Fig. 4; See page 21, lines 9-14); and
- a second logical processor (i.e., MMI Processor 322 of Fig. 3), coupled to the controller (actually, said MMI Processor being coupled to said GSM ULPD via GPIO 321 in Fig. 3), to handle the first SMI (i.e., said waking up process) after the wake-up signal is received from the first logical processor (See page 16, line 28 through page 17, line 2).

Dale does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by

Nalawadi, for said first and second processors (i.e., GSM and MMI Processors), as disclosed by Dale, for the advantage of providing a dual-processor (i.e., multiprocessor) capability for executing multiple-tasks in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

*Referring to claim 41*, Dale teaches that handling the first SMI (i.e., initiating signal for waking up process) with the first logical processor (i.e., GSM Processor 312 of Fig. 3; See page 20, lines 15-23) comprises

- executing the default SMI handler (i.e., instructions being executed by said GSM Processor at Step 490 in Fig. 4) with the first logical processor (i.e., said GSM Processor; See page 21, lines 9-14).

14. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] in view of Nalawadi [US 2003/0009654 A1] as applied to claims 40 and 41 above, and further in view of Rankin [US 5,613,071 A].

*Referring to claim 42*, Dale, as modified by Nalawadi, discloses all the limitations of the claim 42, except that does not expressly teach that the first memory location is 1k aligned.

Rankin discloses a method for providing remote memory access in a massively parallel data processing system (See Abstract), wherein an atomic operation for said remote memory access comprising:

- a first memory address (i.e., said AOM Region) is 4k aligned (See col. 14, lines 14-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said atomic operation, as disclosed by Rankin, in said apparatus (i.e., cellular communication device), as disclosed by Dale, as modified by Nalawadi, for the advantage of providing support for said atomic operations on remote data through said first memory address being aligned (i.e., AOM memory; See Rankin, col. 14, lines 12-13).

Dale, as modified by Nalawadi and Rankin, does not expressly teach that said first memory location is aligned in 1k instead of 4k.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have set up said alignment in 1k, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art<sup>\*</sup>. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

5

15. Claims 50 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dale [GB 2 382 180] as applied to claims 1, 3-5, 45, and 47-49 above, and further in view of Nguyen [US 2002/0099893 A1].

Referring to claim 50, Dale discloses all the limitations of the claim 50, except that does not teach the code at the first memory address is SMI handling code.

Nguyen discloses a system for handling of system management interrupts in a multiprocessor computer system (See Abstract), wherein

- code (i.e., Operating code for SMI handler of Processor 12c in Fig. 1) at a first memory address (i.e., memory location for said Operating code) is SMI handling code (i.e., software SMI handler; See paragraphs [0005] and [0019]).

15

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said handling of system management interrupts (i.e., software SMI handling), as disclosed by Nguyen, in said system, as disclosed by Dale, for the advantage of providing said handling of SMIs for said system (i.e., multiprocessor computer system) using only one or subset of processors (See Nguyen, paragraph [0010]).

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Referring to claim 51, Dale teaches

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<sup>\*</sup> Applicants' disclosure on page 13, paragraph [0038] states that the Applicants' invention is also picking up an optimum value from 1k, 4k, or other aligned memory address range without any particular purpose.

- the wake-up signal (i.e., interrupt signal for waking up MMI Processor 322 of Fig. 3) is a vector (i.e., processor interrupt signal inherently anticipates the claimed subject matter "vector based") containing the first memory address (i.e., interruption signal generated for said MMI Processor; See page 18, line 27 through page 19, line 4).

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16. Claim 60 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen [US 2002/0099893 A1] as applied to claims 26-33, 35-38, 54-59, and 61 above, and further in view of Nalawadi [US 2003/0009654 A1].

Referring to claim 60, Nguyen discloses all the limitations of the claim 60, except that  
10 does not teach that the first and second processors are logical processors.

Nalawadi discloses a computer system having a single processor equipped to serve as multiple logical processors (See Abstract), wherein

- a physical processor (i.e., Intel® Pentium® Family Processor, e.g., Intel® Pentium® 4 Processor; See paragraph [0006], lines 1-7) serving as a first and second logical  
15 processors (i.e., multiple logical processors; See paragraph [0006], lines 7-9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said first and second logical processors, as disclosed by Nalawadi, for said first and second processors (i.e., Processors 12 in Fig. 1), as disclosed by Nguyen, for the advantage of providing a multiprocessor capability for executing multiple-tasks  
20 in parallel using a single physical processor (See Nalawadi, paragraphs [0006]-[0007]).

#### ***Allowable Subject Matter***

17. Claims 12-25 are allowed.

18. Claims 8-11, 34, 39, 43, 44, 52, and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter:

5 With respect to claim 8, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second processor comprises executing the default SMI handler, which is located at the first memory address.

The claims 9-11 are dependent claims of the claim 8.

10 With respect to claim 12, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that executing code at a first memory location with a first processor in response to the first SMI; and executing the code from the first memory location with the second processor, in response to the first SMI after awakening the second processor.

15 The claims 13-25 are dependent claims of the claim 12.

With respect to claim 34, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that the second processor executes the SMI code to handle the SMI for the second processor, if the SMI is software generated.

20 With respect to claim 39, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that returning the target SMBase of the SMI handler to the first SMBase after executing the SMI code to handle the SMI for the second processor.

With respect to claim 43, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second logical processor comprises executing the default SMI handler with the second logical processor.

The claim 44 is a dependent claim of the claim 43.

5           With respect to claim 52, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that handling the first SMI with the second processor after receiving the wake-up signal comprising setting a pointer to a second memory address.

The claim 53 is a dependent claim of the claim 52.

10

### ***Response to Arguments***

20.     Applicants' arguments filed 12<sup>th</sup> of July 2006 have been fully considered but they are not persuasive.

15           *In response to the Applicants' argument with respect to the Specification Objection* (See paragraph 2 of the Non-Final Office Action mailed on 10<sup>th</sup> of April 2006; hereinafter the prior Office Action) in the Response page 13, lines 3-14, it had been fully discussed in the prior Office Action on page 28, and the Examiner further reconsiders.

20           However, the Examiner respectfully disagrees with the Applicants' argument, and thus, maintains the Specification Objection in light of the Argument Response in the prior Office Action.

Therefore, the specification requires the arrangement of "BRIEF SUMMARY OF THE INVENTION" before "BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS" in the specification on page 4.

*In response to the Applicants' argument with respect to "... Applicant's claim 1 includes, 'the wake-up signal references a first memory address of a default SMI handler.' Dale does not disclose referencing a first memory address of a default SMI handler. ... However, there is no suggestion or reference in Dale that either the RADIO-ON signal or the interrupt generated by the GPIO unit references a memory address of a default SMI handler. ..."* in the Response page 14, lines 8-19, and page 15, lines 7-13, the Examiner respectfully disagrees.

In contrary to the Applicants' argument, Dale teaches the wake-up signal (i.e., interrupt signal for waking up MMI Processor) references (i.e., fetches) a first memory address of a default SMI handler (i.e., memory element having instructions in Memory 350 in Fig. 3, which is executed by said GSM Processor at Step 490 in Fig. 4; See Dale, page 21, lines 9-14). Thus, the Applicants' argument on this point is not persuasive.

*In response to the Applicants' argument with respect to "... In contrast, applicant's claims 26, 32, and 54 include limitations similar to executing a SMI handler or SMI code on a first processor and executing the SMI handler or the SMI code on a second processor. Unlike execution of SMI code on one processor with parameter passing from other processors, applicant's claims include execution of the SMI handler or SMI code on both the first and the second processor. ..."* in the Response page 15, line 14 through page 16, the end of the lines, the Examiner respectfully disagrees.

In fact, it is noted that the features upon which applicants rely (i.e., (1) executing a SMI handler or SMI code on a first processor and executing the SMI handler or the SMI code on a second processor, or (2) execution of the SMI handler or SMI code on both the first and the second processor) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In other words, in the exemplary claim 26, the claim recites "executing a SMI handler to handle a SMI **for** a first processor; and executing the SMI handler to handle the SMI **for** a second processor." However, the claim is not read the Applicants' assertion, i.e., (1) executing a SMI handler or SMI code **on** a first processor and executing the SMI handler or the SMI code **on** a second processor, or (2) execution of the SMI handler or SMI code **on both** the first and the second processor.

Thus, the Applicants' argument on this point is not persuasive.

### ***Conclusion***

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

- 5 Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you
- 10 would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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CEL/

